UNITED STATES PATENT AND TRADEMARK OFFICE

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EXAMINER
HSU, JONI

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 08/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

<table>
<tr><td rowspan="2">Office Action Summary</td><td>Application No.</td><td>Applicant(s)</td></tr>
<tr><td>10/759,504</td><td>MEHTA ET AL.</td></tr>
<tr><td></td><td>Examiner</td><td>Art Unit</td></tr>
<tr><td></td><td>Joni Hsu</td><td>2628</td></tr>
</table>

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>02 June 2006</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-56</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-56</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

1.   Applicant's arguments with respect to claims 1-56 have been considered but are moot in view of the new ground(s) of rejection.

2.   Applicant's arguments, see pages 14-15, filed June 2, 2006, with respect to the rejection(s) of claim(s) 1-56 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Frank (US006499072B1).

3.   Applicant argues that the present application and the Bogin patent (US006157397A) were both owned by Intel Corporation at the time of invention of the present application, and Bogin is understood to potentially qualify as prior art only under the provisions of 35 U.S.C. 102(e). Therefore, Bogin cannot properly be relied upon to reject the claims (pages 14-15).

        In reply, the Examiner agrees. However, new grounds of rejection are made in view of Frank.

Claim Rejections - 35 USC § 101

4.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or
> composition of matter, or any new and useful improvement thereof, may obtain a patent
> therefor, subject to the conditions and requirements of this title.

5.   Claims 1-14 and 29-42 are rejected under 35 U.S.C. 101 because the claimed invention is

directed to non-statutory subject matter.

Claims 1-14 are directed to a method of determining buffer management information, but

do not set forth an application of the method to produce a tangible result (i.e. using the result

(buffer management paramerters) to control the buffer level). The claimed invention as a whole

must accomplish a practical application. That is, it must produce a "useful, concrete and tangible

result (*State Street*, 149 F.3d at 1373, 47 USPQ2d at 1601-02). The tangible requirement

requires that the claim must set forth a practical application of the 101 judicial exception to

produce a real-world result (*Benson*, 409 U.S. at 71-72, 175 USPQ at 676-77). See MPEP 2106

II A. Since there is no tangible result recited in these claims, these claims are directed to non-

statutory subject matter.

Claims 29-42 are directed to an **article** comprising a **storage** medium which stores

computer-executable instructions. Claims to computer-related inventions that are clearly

nonstatutory fall into the same general categories as nonstatutory claims in other arts, namely

natural phenomena and abstract ideas or laws of nature which constitute "descriptive material."

Abstract ideas, or the mere manipulation of abstract ideas, are not patentable. "Functional

descriptive material" consists of **computer programs** which impart functionality when

employed as a computer component. Descriptive material is nonstatutory when claimed as

descriptive material *per se*. In order for functional descriptive material to be statutory, it must be

recorded on some **computer**-readable medium so that it becomes structurally and functionally

interrelated to the medium, since use of technology permits the function of the descriptive

material to be realized (*In re Lowry*, 32 F.3d 1579, 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed.

Cir. 1994)). See MPEP 2106 IV B1. Therefore, in order for the claims to be statutory, they must

instead be directed to a **computer program product** comprising a **computer readable** medium

which stores computer-executable instructions.

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or
> described as set forth in section 102 of this title, if the differences between the subject
> matter sought to be patented and the prior art are such that the subject matter as a whole
> would have been obvious at the time the invention was made to a person having ordinary
> skill in the art to which said subject matter pertains. Patentability shall not be negatived
> by the manner in which the invention was made.

7.   The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness
      or nonobviousness.

8.   Claims 1-6, 10-20, 24-34, 38-48, and 52-56 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Wang (US005953020A) in view of Frank (US006499072B1).

9.   With regard to Claim 1, Wang describes a method of determining buffer management

information for a data processing system (*display FIFO memory management system*, Col. 3,

lines 47-53) comprising determining a buffer drain rate based on a first display mode of the data

processing system (*for each given display mode, the draining rate of the display FIFO memory*

for a screen refresh is a constant value, Col. 9, lines 24-31); and calculating one or more buffer

management parameters based on at least the buffer drain rate (*drain rate determinator 80*

includes a counter/timer precision determinator 84 that varies the resolution of the counter/time

82 dependent upon the determined constant drain rate information, Col. 5, lines 58-61).

However, Wang does not teach determining a latency parameter based on a first system

configuration of the data processing system, the latency parameter representing a latency time

amount between a display data request and delivery of display data to a display buffer; and

calculating one or more buffer management parameters based on at least the latency parameter.

According to the disclosure of this application, determining a latency parameter entails

determining the amount of time that the display engine has to wait before it is able to access the

memory [0015-0016]. Frank discloses determining the delay that is the rate at which data is able

to be obtained for a memory request from a frame buffer (Col. 4, lines 11-13, 53-62). The delay

is determined so that data collisions do not occur over the memory read backbone (Col. 2, lines

54-56). Collisions occur as a result of the amount of data delivered by the parallel access to

system and local memory exceeding the data throughput capacity of the buses providing the data

transport from the memory controller to the clients (Col. 1, lines 32-41), and this is considered to be a system configuration. Therefore, Frank discloses a method of determining buffer management information for a data processing system comprising determining a latency parameter based on a first system configuration of the data processing system, the latency parameter representing a latency time amount between a display data request and delivery of display data to a display buffer; and calculating one or more buffer management parameters based on at least the latency parameter (*the data issue delay data 24 indicates, for example, the amount of delay that the sequencer 20 needs to provide for adjusting data read commands over the channels from the frame buffer 22 to allow all of the data from the bus to be transferred over the memory read backbone 25*, Col. 3, lines 7-17).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Wang to include determining a latency parameter based on a first system configuration of the data processing system, the latency parameter representing a latency time amount between a display data request and delivery of display data to a display buffer; and calculating one or more buffer management parameters based on at least the latency parameter as suggested by Frank because Frank suggests that the buffer management parameter must be based on the latency parameter in order to avoid collisions from occurring which create an efficiency problem and potential data throughput bottlenecks (Col. 2, lines 54-56; Col. 1, lines 32-41).

10. With regard to Claim 2, Wang describes determining a buffer fill rate based on a buffer configuration (*the emulation of the drain and fill time of display FIFO memory 70 is*

accomplished by determining the number of memory clock cycles based on the stored displayed mode data, Col. 8, lines 3-8; Col. 9, lines 26-31); and calculating at least one of the one or more buffer management parameters based on the buffer fill rate (*generates the display memory read request signal 62 based on the emulation of the drain and fill time of the display FIFO memory 70*, Col. 5, lines 1-3).

11.   With regard to Claim 3, Wang describes calculating at least one of the one or more buffer management parameters based on a buffer size (*read and write pointers can be compared to determine how many display FIFO entries are leftover in the display FIFO*, Col. 4, lines 22-28; *compares the translated read/write pointer information to generate a display memory read request signal 62*, Col. 4, lines 38-42).

12.   With regard to Claim 4, Wang describes that the one or more buffer management parameters comprise a watermark level (Col. 6, lines 14-17).

13.   With regard to Claim 5, Wang describes that the watermark level comprises a lower bound of a desired watermark level range (*low watermark threshold value*, Col. 9, lines 17-23).

14.   With regard to Claim 6, Wang describes that the watermark level comprises an upper bound of a desired watermark level range (*high watermark*, Col. 9, lines 10-16).

15.   With regard to Claim 10, Wang describes detecting a change from the first display mode

to a second display mode; and calculating at least one of the one or more buffer management

parameters based on the second display mode (*check whether the display mode information*

entered in block 128 has changed, if the display mode information has changed, a new drain rate

is determined, Col. 8, lines 44-50).

16.   With regard to Claim 11, Wang describes detecting a change from the first system

configuration to a second system configuration (*accommodate varying screen display modes*

such as if a user wishes to connect a different screen that may have higher resolution, Col. 5,

lines 53-57); and calculating at least one of the one or more buffer management parameters

based on the second system configuration (*programmable FIFO emulator 72 receives the drain*

rate data and resolution parameter data 86 and stores the drain rate in register 74 and

programs the programmable counter/timer 82 accordingly, programmable FIFO emulator 72

predicts the number of entries left in the display FIFO memory 70 before a complete FIFO

memory drain occurs, Col. 6, lines 7-13).

17.   With regard to Claim 12, Wang does not teach that the latency parameter represents a

maximum expected latency time amount for the first system configuration of the data processing

system. According to the disclosure of this application, determining the maximum expected

latency time amount is the delay for the maximum burst length, and the maximum burst length

value is at the threshold of the buffer so that the buffer does not overflow [0016, 0017, 0020].

Frank discloses determining the delay that is the rate at which data is able to be obtained for a

memory request from a frame buffer (Col. 4, lines 11-13, 53-62). The delay is determined

according to the threshold of the buffer to ensure that the buffer does not overflow (*Data issue*

rate regulator 16 receives the threshold 28 to determine whether a delay is necessary to avoid

data collision. If the number of entries that are filled is greater than the threshold, and a gain

factor associated with that number of entries indicates that a delay is required, and the issue day

data 24 is generated indicating the amount of delay required, Col. 4, line 63-Col. 5, line 17; Col.

2, lines 47-51). The delay is determined so that data collisions do not occur over the memory

read backbone (Col. 2, lines 54-56). Collisions occur as a result of the amount of data delivered

by the parallel access to system and local memory exceeding the data throughput capacity of the

buses providing the data transport from the memory controller to the clients (Col. 1, lines 32-41),

and this is considered to be a system configuration. Therefore, the latency parameter represents

a maximum expected latency time amount for the first system configuration of the data

processing system. This would be obvious for the same reasons given in the rejection for Claim

1.

18.   With regard to Claim 13, Wang describes that the first display mode is characterized by

at least one of a first refresh rate (*display modes will dictate the refresh rate*, Col. 4, lines 16-18),

a first display resolution (*accommodate varying screen display modes such as if a user wishes to*

connect a different screen that may have higher resolution, Col. 5, lines 53-57), and a first color

depth (*display mode data includes color depth data*, Col. 10, lines 19-21).

19.   With regard to Claim 14, Wang does not teach that the first system configuration is

characterized at least by a buffer memory type. However, Frank discloses that the first system

configuration is characterized at least by a buffer memory type (*requesting data from the frame*

buffer, Col. 1, lines 32-39).

It would have been obvious to one ordinary skill in the art at the time of invention by

applicant to modify the device of Wang so that the first system configuration is characterized at

least by a buffer memory type as suggested by Frank because Frank suggests that the apparatus

needs to know what type of memory the memory request is being made to in order to determine

whether a delay is necessary (Col. 5, lines 17-40).

20.   With regard to Claim 15, Wang describes an apparatus comprising a display part (14,

Figure 1) which directs movement of display data, the display part including a buffer (30) to

store display data to be displayed on a display screen (40) (Col. 4, lines 2-16); and a data

computing system configured to calculate one or more buffer management parameters based on a

buffer drain rate based on a first display mode; wherein the buffer drain rate represents a rate at

which the display data is read from the buffer (Col. 9, lines 26-31; Col. 5, lines 58-61).

However, Wang does not teach calculating one or more buffer management parameters

based on a latency parameter based on a first system configuration; wherein the latency

parameter represents a latency time amount between a display data request and delivery of

display data to the buffer. According to the disclosure of this application, determining a latency

parameter entails determining the amount of time that the display engine has to wait before it is

able to access the memory [0015-0016]. Frank discloses determining the delay that is the rate at

which data is able to be obtained for a memory request from a frame buffer (Col. 4, lines 11-13,

53-62). The delay is determined so that data collisions do not occur over the memory read

backbone (Col. 2, lines 54-56). Collisions occur as a result of the amount of data delivered by

the parallel access to system and local memory exceeding the data throughput capacity of the

buses providing the data transport from the memory controller to the clients (Col. 1, lines 32-41),

and this is considered to be a system configuration. Therefore, Frank discloses a method of

determining buffer management information for a data processing system comprising

determining a latency parameter based on a first system configuration of the data processing

system, the latency parameter representing a latency time amount between a display data request

and delivery of display data to a display buffer; and calculating one or more buffer management

parameters based on at least the latency parameter (Col. 3, lines 7-17). This would be obvious

for the same reasons given in the rejection for Claim 1.

21.   With regard to Claims 16-20 and 24-28, these claims are similar in scope to Claims 2-6

and 10-14 respectively, and therefore are rejected under the same rationale.

22.   With regard to Claim 29, Claim 29 is similar in scope to Claim 1, except that Claim 29 is

for an article comprising a storage medium which stores computer-executable instructions, the

instructions causing a computer to perform the method of Claim 1. Wang describes an article

comprising a storage medium which stores computer-executable instructions, the instructions

causing a computer to perform the method (Col. 5, lines 26-39). Therefore, Claim 29 is rejected

under the same rationale as Claim 1.

23.   With regard to Claims 30-34, 38-48, 52-56, these claims are similar in scope to Claims 2-

6, 10-20, and 24-28 respectively, and therefore are rejected under the same rationale.

24.   Claims 7, 9, 21, 23, 35, 37, 49 and 51 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Wang (US005953020A) and Frank (US006499072B1) in view of Shimomura

(US006600492B1).

25.   With regard to Claim 7, Wang and Frank are relied upon for the teachings as discussed

above relative to Claim 1.

       However, Wang and Frank do not teach that the one or more buffer management

parameters comprise a burst length. However, Shimomura describes that the one or more buffer

management parameters (Col. 16, lines 27-37) comprise a burst length (Col. 21, lines 4-23).

       It would have been obvious to one of ordinary skill in the art at the time of invention by

applicant to modify the devices of Wang and Frank so that the one or more buffer management

parameters comprise a burst length as suggested by Shimomura because Shimomura suggests

that adjusting the burst length can reduce the amount of power consumption (Col. 21, lines 6-11).

26.   With regard to Claim 9, Wang does not teach that the burst length comprises an upper

bound of a desired burst length range. However, Shimomura describes that the burst length

comprises an upper bound of a desired burst length range (Col. 21, lines 12-23, *threshold value*

is updated by using a maximum number of access cycles obtained from the burst-length table

13500, Col. 21, lines 33-40).

It would have been obvious to one of ordinary skill in the art at the time of invention by

applicant to modify the device of Wang so that the burst length comprises an upper bound of a

desired burst length range as suggested by Shimomura because Shimomura suggests that the

larger the burst length, the more the power consumption is reduced (Col. 21, lines 6-11), and

therefore the system needs to know the upper bound of the desired burst length range.

27.   With regard to Claims 21 and 23, these claims are similar in scope to Claims 7 and 9

respectively, and therefore are rejected under the same rationale. With regard to Claims 35 and

37, these claims are also similar in scope to Claims 7 and 9 respectively, and therefore are also

rejected under the same rationale. With regard to Claims 49 and 51, these claims are similar in

scope to Claims 21 and 23 respectively, and therefore are rejected under the same rationale.

28.   Claims 8, 22, 36, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Wang (US005953020A), Frank (US006499072B1), and Shimomura (US006600492B1) in view

of Ashburn (US006628292B1).

29.   With regard to Claim 8, Wang, Frank, and Shimomura are relied upon for the teachings

as discussed above relative to Claim 7.

However, Wang, Frank, and Shimomura do not teach that the burst length comprises a

lower bound of a desired burst length range. However, Ashburn describes that the burst length

comprises a lower bound of a desired burst length range (*minimum burst length*, Col. 2, lines 35-46).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Wang, Frank, and Shimomura so that the burst length comprises a lower bound of a desired burst length range as suggested by Ashburn because Ashburn suggests that the system needs to know the minimum burst length that can create a free command cycle in order to increase memory bandwidth (Col. 2, lines 24-27, 36-38).

30.   With regard to Claims 22 and 36, these claims are both similar in scope to Claim 8, and therefore are rejected under the same rationale. With regard to Claim 50, Claim 50 is similar in scope to Claim 22, and therefore is rejected under the same rationale.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER